System and Method for Separating Exception Vectors in a Multiprocessor Data Processing System

Abstract of the Disclosure

A system and method is provided for uniquely handling exception an interrupts in at least two different processors in a multiprocessor system. Initially, the memory address identified in a common exception vector table is written to contain an instruction which copies the current version of an IRQ-mode banked register into the program counter of the processor for subsequent execution. Next, each processor initializes independent IRQ-mode registers to contain the respective addresses for their individual IRQ handler routines. Upon receipt of an interrupt request or other exception, the processor receiving the request changes to an IRQ-mode, resulting in at least one register change from a normal register to the previously initialized IRQ-mode register. Next, the processor looks in the exception vector table for the appropriate interrupt handler address location and jumps to the identified memory location. Correspondingly, the processor executes the instruction at this location and moves a processor-specific IRQ-mode banked register into the program counter. Next, the processor jumps to the address location for the calling processor's unique IRQ handling routine, written in the IRQ-mode banked register.

Figures